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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/796,111	03/10/2004	Dean A. Klein	M4065.0959/P959	2460

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EXAMINER	
LUU, PHO M	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 11/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/796,111	KLEIN DEAN A	
	Examiner	Art Unit	
	Pho M Luu	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-85* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *12-44 and 61* is/are allowed.

6)☒ Claim(s) *1-8,45-50,62-65,69-77 and 81-85* is/are rejected.

7)☒ Claim(s) *9-11,51-60,66-68 and 78-80* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *06/10/04; 06/21/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Search History*.

DETAILED ACTION

Specification

1. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

2. The abstract of the disclosure is objected to because it uses the phrase "**In a memory system**" in line 1, "**As a result**" in line 4, **"For example"** in line 5 and **"Also"** in line 7, which is implied. Correction is required. See MPEP § 608.01(b).

Information Disclosure Statement

3. Acknowledgment is made of applicant's Information Disclosure Statement (IDS) Form PTO-1449, filed 21 June 2004. The information disclosed

therein was considered.

Acknowledgment is made of applicant's Information Disclosure Statement (IDS) Form PTO-1449, filed 10 June 2004. The information disclosed therein was considered.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-8, 50, 62-65, 74-77 are rejected under 35 U.S.C. 102(b) as being anticipated by Kuddes. (US. 5,418,920).

Regarding claim 1, Kuddes in Figure 2 discloses a refresh circuit (10) that controls a refresh operation of a memory array, the refresh circuit indicating when the refresh operation is complete (see column 13, lines 10-15).

With respected to claim 2, Kuddes in Figure 2 disclosed the refresh circuit includes a refresh counter (22).

With respected to claim 3, Kuddes in Figure 2 disclosed the refresh circuit comprises a refresh complete circuit (30) for indicating when the refresh operation is complete (see column 13, lines 10-15).

With respected to claim 4, Kuddes in Figure 2 disclosed the refresh circuit provides a signal (the output of 30) indicating when the refresh operation is completed (see column 13, lines 10-15).

Regarding claim 5, Kuddes in Figure 1-2 discloses a memory device comprising a memory array (4, Figure 1); and a refresh circuit (10, Figure 2) that control a refresh operation of the memory array, the refresh circuit indicating when the refresh operation is complete (see column 13, lines 10-15).

With respected to claim 6, Kuddes in Figure 2 disclosed the refresh circuit includes a refresh counter (22).

With respected to claim 7, Kuddes in Figure 2 disclosed the refresh circuit comprises a refresh complete circuit (30) for indicating when the refresh operation is complete (see column 13, lines 10-15).

With respected to claim 8, Kuddes in Figure 2 disclosed the refresh circuit provides a signal (the output of 30) indicating when the refresh operation is completed (see column 13, lines 10-15).

Regarding claim 50, Kuddes in Figure 2 discloses a method of refreshing memory comprising performing a burst self-refresh operation (performed by counter 22 in Figure 2) on a memory array; and

providing a refresh completed signal when the burst self-refresh operation has been completed (performed by 30, Figure 2).

Regarding claim 62, Kuddes in Figure 1-2 discloses integrated circuit comprising:

a memory device (Figure 1) comprising a memory array (4, Figure 1) and

a refresh circuit (16, 22, 30, Figure 2) that control a refresh operation of the memory array, the refresh circuit indicating when the refresh operation is complete (performed by 30, Figure 2, also; see column 13, lines 10-15).

With respected to claim 63, Kuddes in Figure 2 disclosed the refresh circuit includes a refresh counter (22).

With respected to claim 64, Kuddes in Figure 2 disclosed the refresh circuit comprises a refresh complete circuit (30) for indicating when the refresh operation is complete (see column 13, lines 10-15).

With respected to claim 65, Kuddes in Figure 2 disclosed the refresh circuit provides a signal (the output of 30) indicating when the refresh operation is completed (see column 13, lines 10-15).

Regarding claim 74, Kuddes in Figure 1-2 discloses a processor system comprising:

a processor (6, Figure 1) and a memory device (10, Figure 2) comprising a memory array (4, Figure 1) and a refresh (16, 22, 30, Figure 2) circuit that controls a refresh operation of the memory array, the refresh circuit indicating when the refresh operation is completed (see column 13, lines 10-15).

With respected to claim 75, Kuddes in Figure 2 disclosed the refresh circuit includes a refresh counter (22).

With respected to claim 76, Kuddes in Figure 2 disclosed the refresh circuit comprises a refresh complete circuit (30) for indicating when the refresh operation is complete (see column 13, lines 10-15).

With respected to claim 77, Kuddes in Figure 2 disclosed the refresh circuit provides a signal (the output of 30) indicating when the refresh operation is completed (see column 13, lines 10-15).

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 45-49, 69-73 and 81-85 are rejected under 35 U.S.C. 102(b) as being anticipated by Ware et al. (US. 5,446,696).

Regarding claim 45, Ware et al in Figure 5 disclosed a memory device comprising:

refresh circuitry (545, Figure 5) that controls a refresh operation in a memory device (500, Figure 5); and

a sensor (570, Figure 5) that senses an environmental condition of the memory device; wherein the refresh circuit (545, 565, Figure 5) initiating the refresh operation partially in response to the environmental condition sensed by the sensor (570, Figure 5).

With respected to claim 46-49, Ware et al in Figure 5 disclosed the sensor is a temperature sensor (570) and located outside the memory system (see Figure 5).

Regarding claim 69, Ware et al in Figure 5 disclosed a memory device comprising:

refresh circuitry (545, Figure 5) that controls a refresh operation in a memory device (500, Figure 5); and

a sensor (570, Figure 5) that senses an environmental condition of the memory device; wherein the refresh circuit (545, 565, Figure 5) initiating the refresh operation partially in response to the environmental condition sensed by the sensor (570, Figure 5).

With respected to claim 70-73, Ware et al in Figure 5 disclosed the sensor is a temperature sensor (570) and located outside the memory system (see Figure 5).

Regarding claim 81, Ware et al in Figure 5 disclosed a memory device comprising:

refresh circuitry (545, Figure 5) that controls a refresh operation in a memory device (500, Figure 5); and

a sensor (570, Figure 5) that senses an environmental condition of the memory device; wherein the refresh circuit (545, 565, Figure 5) initiating the refresh operation partially in response to the environmental condition sensed by the sensor (570, Figure 5).

With respected to claim 82-85, Ware et al in Figure 5 disclosed the sensor is a temperature sensor (570) and located outside, inside and location of the memory system (see Figure 5).

Allowable Subject Matter

8. Claims 9-11, 51-60, 66-68, 78-80 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 9, the prior art of record do not disclose or suggest the control logic circuit providing a first control signal to the refresh circuit.

Regarding claim 51, the prior art of record do not disclose or suggest a determining a pre-refresh mode of the memory array before performing.

Regarding claim 57, the prior art of record do not disclose or suggest initiating the refresh operation at a certain rate.

Regarding claim 66, the prior art of record do not disclose or suggest a control logic circuit that control an operation of the memory array.

Regarding claim 78, the prior art of record do not disclose or suggest a control logic circuit providing a first control signal to the refresh circuit.

10. Claims 12-44 and 61 are allowed.

The following is an examiner's statement of reasons for allowance:

There is no teaching or suggestion in the prior art to: "a combining circuit that combines the refresh completed signal from the memory device to obtain a combined refresh completed signal" as claimed in the independent claim 12 and independent claim 24; or

"a micro-controller for controlling an operation of the power management circuit" as claimed in the independent claim 35 and independent claim 42; or

"combining the refresh signals to obtain a combined refresh completed signal" as claimed in the independent claim 61; or

Conclusion

11. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Pho M. Luu whose telephone number is 571.272.1876. The examiner can normally be reached on M-F 8:00AM – 5:00PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's Supervisor, Richard Elms, can be reached on 571.272.1869. The official fax number for the organization where this application or proceeding is assigned is 703.872.9306 for all official communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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28 October 2004

Pho M. Luu
Patent Examiner
Art Unit 2824